

Claims

1. Apparatus including

a first device having a plurality of network input interfaces and a plurality of network output interfaces, said first device including a packet information extractor coupled to at least one said network input interface;

a second device coupled to said packet information extractor, said second device capable of generating packet forwarding information and output port information responsive to an output of said packet information extractor; and

an information link, coupled to said first device and said second device.

2. Apparatus as in claim 1, wherein

said first device includes a packet rewriter coupled to at least one said network output interface; and

said second device includes a packet rewrite generator coupled to said first device, said packet rewrite generator disposed for generating said packet forwarding information and output port information;

wherein said packet rewrite element is responsive to said packet rewrite generator.

3. Apparatus as in claim 1, including a packet buffer memory coupled

to said first device.

1 4. Apparatus as in claim 1, wherein said first device consists of a circuit
2 integrated into a single monolithic semiconductor circuit.

3
4 5. Apparatus as in claim 1, wherein said second device consists of a
5 circuit integrated into a single monolithic semiconductor circuit.

6
7 6. Apparatus as in claim 1, wherein
8 said first device consists of a circuit integrated into a single monolithic
9 semiconductor circuit; and

10 said second device consists of a circuit integrated into a single monolithic
11 semiconductor circuit.

12
13 7. Apparatus as in claim 1, including a rewrite table including said re-
14 write information.

15
16 8. Apparatus as in claim 7, wherein said first device includes said re-
17 write table.

18
19 9. Apparatus as in claim 7, wherein said second device includes an ad-
20 dress pointing into said rewrite table, wherein said address can be forwarded to said first
21 device.

1 10. Apparatus including

2 a first device having at least one input interface and at least one output in-
3 terface, said first device including an information extractor having an input coupled to a
4 packet received from said input interface and having an output coupled to a first memory;
5 and

6 a second device including a decision generator having an input coupled to
7 said first device, and having an output coupled to said first device;

8 wherein said first device is responsive to a forwarding treatment from said
9 second device to determine a set of said output interfaces on which to couple said packet.

10
11 11. Apparatus as in claim 10, wherein

12 said forwarding treatment includes packet rewrite information; and

13 said first device is responsive to said packet rewrite information to rewrite
14 said packet before coupling said packet to said set of output interfaces.

15
16 12. Apparatus as in claim 10, wherein said forwarding treatment in-
17 cludes at least one action relating to accounting.

18
19 13. Apparatus as in claim 10, wherein said forwarding treatment is re-
20 sponsive to information regarding access control.

1 14. Apparatus as in claim 10, wherein said forwarding treatment is re-
2 sponive to information regarding class of service or quality of service.

3
4 15. Apparatus as in claim 10, wherein said forwarding treatment is re-
5 sponive to information regarding parsing, extracting and encoding the packet informa-
6 tion passed from said first device to said second device so as to minimize the amount of
7 said information forwarded between said first device and said second device.

8
9 16. Apparatus as in claim 10, wherein said forwarding treatment is re-
10 sponive to said packet information memory.

11
12 17. Apparatus as in claim 10, wherein said first device consists of a cir-
13 cuit integrated into a single monolithic semiconductor circuit.

14
15 18. Apparatus as in claim 10, wherein said second device consists of a
16 circuit integrated into a single monolithic semiconductor circuit.

17
18 19. A device integrated into a single monolithic semiconductor circuit,
19 said device including

20 at least one input interface and at least one output interface;

21 an information extractor having an input coupled to a packet received from
22 said input interface, and having an output coupled to a packet information memory;

1 an input coupled to a forwarding treatment memory;
2 said device being responsive to said forwarding treatment memory to de-
3 termine a set of said output interfaces on which to couple said packet.

4
5 20. Apparatus as in claim 19, including
6 a second device coupled to said packet information memory;
7 a decision generator in said second device having an input coupled to said
8 packet information memory, and having an output coupled to a forwarding treatment
9 memory;

10 said first device being responsive to said forwarding treatment memory to
11 determine a set of said output interfaces on which to couple said packet.

12
13 21. A device integrated into a single monolithic semiconductor circuit,
14 said device including
15 an input coupled to a packet information memory;
16 an output coupled to a forwarding treatment memory; and
17 a decision generator coupled to said packet information memory and to said
18 forwarding treatment memory.

19
20 22. Apparatus as in claim 21, including
21 a packet data device having at least one input interface and at least one out-
22 put interface, said packet data device including an information extractor having an input

6

of the \mathbb{Z}_2 -action on \mathbb{R}^n is given by $(x_1, \dots, x_n) \mapsto (-x_1, \dots, -x_n)$. The quotient space $\mathbb{R}^n / \mathbb{Z}_2$ is homeomorphic to the cone $C(\mathbb{S}^{n-1})$. The quotient map $\pi: \mathbb{R}^n \rightarrow \mathbb{R}^n / \mathbb{Z}_2$ is a \mathbb{Z}_2 -equivariant map. The quotient map π is a \mathbb{Z}_2 -equivariant map. The quotient map π is a \mathbb{Z}_2 -equivariant map.